14. (Amended) A method for fabricating a semiconductor device, as recited in claim 10, wherein the interlayer insulating layer has a first etching rate at least five times as high as a second etching rate of the insulating layer.

18. (Amended) A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the implanting of second impurity ions is performed using boron [or BF_3] with a dose range of about $1x10^{13}$ ions/cm^2 and at an energy range of about 20 keV.

19. (Amended) A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the implanting of third impurity ions is performed using ~~boron fluoride (BF_2)~~ [boron or BF_3] with a dose range of about $5x10^{15}$ ions/cm^2 and at an energy range of about 20 keV.

REMARKS

In the Office Action dated August 15, 2000, the Examiner required a new title. The Examiner rejected claim 14 under 35 U.S.C. § 112, second paragraph, as allegedly containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention. The Examiner rejected claims 1, 10, and 12 under 35 U.S.C. § 112, second paragraph, as being allegedly indefinite for failing to particularly point out and distinctly claim the

subject matter which applicant regards as the invention. The Examiner rejected claims 1-4 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Choi et al. (United States Patent No. 5,654,213) in view of Kashihara et al. (United States Patent No. 5,567,964), rejected claims 5, 6, and 8 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Choi et al. in view of Kashihara et al., and further in view of Kim (UK Patent Application GB 2 257 563 A), rejected claims 7 and 9 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Choi et al. in view of Kashihara et al., and further in view of Mitsui (United States Patent No. 5,296,401), and rejected claims 10-19 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Choi et al. in view of Kashihara et al. and Matsui, and further in view of Ong (Morden MOS Technology, McGraw-Hill, 1986).

The Title

The Examiner has required a new title. In response to this request, Applicants have deleted the original title and have provided a new title of: "METHOD OF FABRICATING A MOS TRANSISTOR WITH DOUBLE SIDEWALL SPACERS IN A PERIPHERAL REGION AND SINGLE SIDEWALL SPACERS IN A CELL REGION." This is substantially the same as the title suggested by the Examiner.

Rejection under 35 U.S.C. § 112, First Paragraph

The Examiner has rejected claim 14 under 35 U.S.C. § 112, second paragraph, as allegedly containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention. In particular, the Examiner has asserted that the specification does not disclose that the interlayer insulating layer have a first etching rate at least five times as high as a second etching rate of the insulating layer, as recited in claim 14. Applicants respectfully traverse this assertion.

Claim 14 does not recite two separate etching steps as the Examiner appears to assert. Rather, claim 14 recites that interlayer insulating layer have a first etching rate at least five times as high as a second etching rate of the insulating layer. This is shown in Applicants' specification on page 17, lines 4-7, which notes that "The interlayer insulating layer 120 is selectively etched (preferably for about five times) with respect to the remaining insulating layer 112a." In other words, the interlayer insulating layer 120 is etched five times as fast as the remaining insulating layer 112a, which means that the etching rate of the interlayer insulating layer 120 is at least five times as fast as the etching rate of the remaining insulating layer 112a.

Thus, Applicants respectfully submit that claim 14 does not contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention. Applicant therefore respectfully

requests that the Examiner withdraw the rejection of claim 14 under 35 U.S.C. § 112, first paragraph.

Rejection under 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected claims 1, 10, and 12 under 35 U.S.C. § 112, second paragraph, as being allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding the rejection of claim 1, Applicants have amended claim 1 to better recite the relationships between the various spacers and gates. In particular, Applicants have amended claim 1 to recite that the spacers are "on lateral sides" of their respective gates.

In particular, in lines 15-16, Applicants refer to the first gate spacers on the lateral side of the third gate. In lines 19-20, Applicants refer to second gate spacers adjacent to the first gate spacers on the lateral side of the second and third gates, respectively. In lines 22-23, Applicants refer to the second spacers on the lateral side of the first spacers of the second gate. In lines 24-25, Applicants refer to the second gate and the first and second spacers. In lines 27-28, Applicants refer to the second spacers on the lateral side of the third gate.

Regarding rejection of claims 10 and 12, Applicants have deleted the word "for," and the extraneous comma, and so have eliminated any lack of clarity in these claims.

Therefore, Applicants respectfully submit that claims 1, 10, and 12 are fully definite and meet the requirements of 35 U.S.C. § 112, second paragraph. Applicants therefore respectfully request that the Examiner withdraw the rejection of claims 1, 10, and 12 as being allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Rejection under 35 U.S.C. § 103(a) based on Choi et al. and Kashihara et al.

The Examiner has rejected claims 1-4 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Choi et al. in view of Kashihara et al. Applicants respectfully traverse this rejection.

Claim 1 recites "forming a first gate in the cell array region, a second gate in the peripheral region, and a third gate in the peripheral circuit region." Neither Choi et al. nor Kashihara et al., alone or in combination, disclose or suggest this feature. In particular, nothing in either Choi et al. nor Kashihara et al. suggests that a first gate be formed in a cell array region.

Claim 1 recites "implanting third impurity ions of a low concentration into a third portion of the semiconductor substrate . . . using the third gate and first gate spacers as a mask, to form a third impurity diffusion region of a second conductivity type." However, as shown in Fig. 12 of Choi et al., when a lightly-doped p⁻ implant takes place, the sidewalls (89 and 90) on the unmasked spacer (70) are stripped off. (See, e.g., Choi et al., column 4, lines 12-17, and Fig. 12.) Thus, Choi et al. cannot disclose "implanting third

impurity ions of a low concentration . . . using the third gate and first gate spacers as a mask," as recited in claim 1.

Claim 1 also recites "implanting fourth impurity ions of a high concentration into a fourth portion of the semiconductor substrate" and "implanting fifth impurity ions of a high concentration into a fifth portion of the semiconductor substrate." Neither Choi et al. nor Kashihara et al., alone or in combination, disclose or suggest this feature. The Examiner has asserted that Choi et al. discloses this feature in it's Figs. 16 and 17. However, a close examination of these drawings and the related disclosure will show that this is not the case.

Fig. 16 of Choi et al. discloses introducing dopant into contact holes to reduce contact resistance. (See, e.g., Choi et al., column 5, lines 43-46, and Fig. 16.) Similarly, Fig. 17 of Choi et al. discloses introducing dopant of a second conductivity type into the contact hole touching the source and drain regions to decrease the contact resistance in the contact areas located within the source and drain regions. (See, e.g., Choi et al., column 5, lines 46-51, and Fig. 17.) However, such doping used to reduce contact resistance is not the same as the high concentration implantation recited in claim 1, nor would it render such high concentration implantation obvious.

More specifically, claim 1 recites "implanting fourth impurity ions of a high concentration into a fourth portion of the semiconductor substrate . . . using the second gate and the first and second spacers as a mask, to form a fourth impurity diffusion region of a first conductivity type." Applicants are uncertain exactly what the Examiner

considers to be the recited second spacer, but it is clear from Fig. 16 of Choi et al. that the uppermost layer in Fig. 16 (unnamed) is used as a mask for the doping of the contact areas, and not any of sidewall spacers 87-90 or gate structures 70 or 75. Thus, Choi et al. does not meet the limitation of claim 1 that the second gate and the first and second spacers be used as a mask.

Similarly, claim 1 recites "implanting fifth impurity ions of a high concentration into a fifth portion of the semiconductor substrate . . . using the third gate and first and second spacers as a mask, to form a fifth impurity diffusion region of a second conductivity type. Again, Applicants are uncertain exactly what the Examiner considers to be the recited second spacer, but it is clear from Fig. 17 of Choi et al. that the uppermost two layers in Fig. 17 (both unnamed) are used as a mask for the doping of the contact areas, and not any of sidewall spacers 87-90 or gate structures 70 or 75. Thus, Choi et al. does not meet the limitation of claim 1 that the third gate and the first and second spacers be used as a mask.

Kashihara et al. does not cure the deficiencies in Choi et al. noted above.

Thus, neither Choi et al. nor Kashihara et al., alone or in combination, disclose or suggest every feature recited in claims 1, 10, and 12. Applicants therefore respectfully request that the Examiner withdraw the rejection of claims 1, 10, and 12 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Choi et al. in view of Kashihara et al.

Rejection under 35 U.S.C. § 103(a) based on Choi et al., Kashihara et al., and Kim

The Examiner has rejected claims 5, 6, and 8 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Choi et al. in view of Kashihara et al., and further in view of Kim. Applicants respectfully traverse this rejection.

Claims 5, 6, and 8 depend from claim 1 and are allowable for at least the reasons given above for claim 1. Kim does not cure the deficiencies in Choi et al. and Kashihara et al. noted above.

Thus, none of Choi et al., Kashihara et al., or Kim, alone or in combination, disclose or suggest every feature recited in claims 5, 6, and 8. Applicants therefore respectfully request that the Examiner withdraw the rejection of claims 5, 6, and 8 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Choi et al. in view of Kashihara et al., and further in view of Kim.

Rejection under 35 U.S.C. § 103(a) based on Choi et al., Kashihara et al., and Mitsui

The Examiner has rejected claims 7 and 9 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Choi et al. in view of Kashihara et al., and further in view of Mitsui. Applicants respectfully traverse this rejection.

Claims 7 and 9 depend from claim 1 and are allowable for at least the reasons given above for claim 1. Mitsui does not cure the deficiencies in Choi et al. and Kashihara et al. noted above.

Thus, none of Choi et al., Kashihara et al., or Mitsui, alone or in combination, disclose or suggest every feature recited in claims 7 and 9. Applicants therefore respectfully request that the Examiner withdraw the rejection of claims 7 and 9 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Choi et al. in view of Kashihara et al., and further in view of Mitsui.

Rejection under 35 U.S.C. § 103(a) based on Choi et al., Kashihara et al., Mitsui, and Ong

The Examiner has rejected claims 10-19 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Choi et al. in view of Kashihara et al. and Matsui, and further in view of Ong (Morden MOS Technology, McGraw-Hill, 1986).

Claims 10-14 depend from claim 1 and are allowable for at least the reasons given above for claim 1. Ong does not cure the deficiencies in Choi et al., Kashihara et al., and Mitsui noted above.

Claim 15 recites "implanting second impurity ions of a low concentration into a third portion of the semiconductor substrate . . . using the gate and first gate spacers as a mask, to form a second impurity diffusion region." However, as shown in Fig. 12 of Choi et al., when a lightly-doped p^- implant takes place, the sidewalls (89 and 90) on the unmasked spacer (70) are stripped off. (See, e.g., Choi et al., column 4, lines 12-17, and Fig. 12.) Thus, Choi et al. cannot disclose "implanting second impurity ions of a low concentration . . . using the gate and first gate spacers as a mask," as recited in claim 15.

Claim 15 also recites "implanting third impurity ions of a high concentration of a second conductivity type, using the gate and the first and second spacers as a mask." None of Choi et al., Kashihara et al., or Matsui, alone or in combination, disclose or suggest this feature. Although the Examiner has not specifically set forth the basis for this rejection, Applicants believe that the Examiner relies upon Figs. 16 and 17 of Choi et al. for this teaching. However, a close examination of these drawings and the related disclosure will show that this is not the case.

Fig. 16 of Choi et al. discloses introducing dopant into contact holes to reduce contact resistance. (See, e.g., Choi et al., column 5, lines 43-46, and Fig. 16.) Similarly, Fig. 17 of Choi et al. discloses introducing dopant of a second conductivity type into the contact hole touching the source and drain regions to decrease the contact resistance in the contact areas located within the source and drain regions. (See, e.g., Choi et al., column 5, lines 46-51, and Fig. 17.) However, such doping used to reduce contact resistance is not the same as the high concentration implantation recited in claim 15, nor would it render such high concentration implantation obvious.

More specifically, claim 15 recites "implanting third impurity ions of a high concentration . . . using the gate and the first and second spacers as a mask." Applicants are uncertain exactly what the Examiner considers to be the recited second spacer, but it is clear from Fig. 16 of Choi et al. that the uppermost layer in Fig. 16 (unnamed) is used as a mask for the doping of the contact areas, and not any of sidewall spacers 87-90 or gate structures 70 or 75. Similarly, the uppermost two layers in Fig. 17 (both unnamed)

are used as a mask for the doping of the contact areas, and not any of sidewall spacers 87-90 or gate structures 70 or 75. Thus, Choi et al. Does not meet the limitation of claim 15 that the gate and the first and second spacers be used as a mask.

None of Kashihara et al., Mitsui, or Ong, cure the deficiencies in Choi et al. noted above.

Claims 16-19 depend from claim 15 and are allowable for at least the reasons given above for claim 1.

Thus, none of Choi et al., Kashihara et al., Mitsui, or Ong, alone or in combination, disclose or suggest every feature recited in claims 10-19. Applicants therefore respectfully request that the Examiner withdraw the rejection of claims 10-19 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Choi et al. in view of Kashihara et al. and Matsui, and further in view of Ong

Claim Amendments

Applicants have amended claims 7 and 18 to eliminate the recitation of BF_3 for use in implanting of the third impurity ions.

Applicants have also amended claims 9 and 19 to indicate that the implanting of fifth impurity ions is performed using boron fluoride (BF_2) rather than boron or BF_3. Applicants note in their specification on page 14, line 5-9 that high concentration p-type impurity ions are implanted into the semiconductor substrate, and that the p-type impurity may include boron (B) or BF_3. This broadly describes the use of boron fluoride (BF_2),

which includes boron, as noted in the specification. Furthermore, given this description, one skilled in the art would understand that boron fluoride (BF_2) may be used as an impurity ion.

Applicants therefore respectfully request that the Examiner enter the claim amendments to claims 7, 9, 18, and 19.

Conclusion

Based on the above amendments and remarks, Applicants respectfully request that the Examiner consider this amendment, enter the listed claim amendments, reconsider and reexamine this application, and issue a Notice of Allowance allowing pending claims 1-19.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Brian C. Altmiller (Reg. No. 37,271) at (703) 715-0870 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully Submitted,
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